AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. (Currently amended) Circuitry comprising:

a voltage regulator comprising a first stage and a second stage, wherein an output of said first stage is coupled to an input of said second stage, wherein current of said second stage is mirrored through a current path to a current mirror driver, said current mirror driver adapted to perform a first Class AB action comprising at least one of sourcing and sinking current from a voltage supply VPP, wherein an output of said current mirror driver is connected to an output of said voltage regulator; [[and]]

a first circuit connected to said current path and adapted to sample current in said current path, wherein during steady state current in said current path, said first circuit provides negligible current to the output of said voltage regulator, and during transient current conditions, said first circuit performs a second Class AB action complementary to said first Class AB action comprising at least one of sinking and sourcing current from the voltage supply VPP;

and wherein said first and second stages both operate from a voltage supply VDD, which is at a lower voltage than VPP.

2. (Original) The circuitry according to claim 1, wherein said first stage comprises a differential stage and said second stage comprises an inverting stage, and said input of said second stage is a gate of an MOS transistor.

3. (Original) The circuitry according to claim 1, wherein the output of said voltage regulator is connected to a capacitance load.

4. (Original) The circuitry according to claim 3, wherein said capacitance load comprises at least one of a wordline and a wordline driver of a memory array.

5. (Currently amended) The circuitry according to claim 1, wherein the output of said first stage is coupled to [[the]] a gate of said second stage without a Miller compensating capacitor.

6. (Original) The circuit according the claim 1, wherein said voltage regulator and said first and second stages form a two pole system based on an anti-Miller principle.

7. (Cancelled)

8. (Currently amended) The circuitry according to claim [[7]] 1, further comprising:

an NMOS transistor M1B whose gate is connected to an input BGREF, whose drain is connected to a node N10, and whose source is connected to a node N11;

a current source I1 connected to said node N11 and which is grounded;

an NMOS transistor M1A whose source is connected to said node N11, whose gate is connected to a node N12, and whose drain is connected via a node N13 to the drain of a PMOS transistor M2A, wherein said PMOS transistor M2A has its gate connected via said node N13 to its drain, and whose source is connected to voltage VDD;

and a PMOS transistor M2B whose gate is connected to the gate of said PMOS transistor M2A, whose drain is connected to said node N10, and whose source is connected to voltage VDD;

and further comprising:

a PMOS transistor M3 whose drain is connected to a node N14, whose source is connected to voltage VDD, and whose gate PG is connected to said first stage at said node N10;

an NMOS transistor M4A whose gate and drain are connected to said node N14, and whose source is grounded;

an NMOS transistor M4B whose drain is connected to a node N15, whose gate is connected to the gate of said NMOS transistor M4A, and whose source is grounded;

an NMOS transistor M4C whose drain is connected to a node N16, whose gate is connected to the gate of said NMOS transistor M4B, and whose source is grounded;

a current source I2, one node of which is connected to said node N16, and another node of which is connected to voltage VDD;

a pair of NMOS transistors M6A and M6B whose gates are connected together and to node N16 and whose sources are grounded, wherein the drain of said NMOS transistor M6A is connected to its gate and the drain of said NMOS transistor M6B is connected to the output of said voltage regulator;

a pair of PMOS transistors M5A and M5B whose gates are connected together and to node N15 and whose sources are connected to VPP, the drain of said PMOS transistor M5A being connected to said node N15, and the drain of said PMOS transistor M5B being connected to the output of said voltage regulator; and

a resistor divider comprising a first resistor R0 connected between the output of said voltage regulator and a node N12, and a second resistor R1 connected between said node N12 and ground;

wherein said first stage comprises said current source I1, said transistors M1A, M1B, M2A and M2B, said second stage comprises said transistor M2, said current path comprises said transistors M4A and M4B,

and said current mirror driver comprises said PMOS transistors M5A and M5B, and said first circuit comprises said NMOS transistors M4C, M6A, M6B and said current source I2.

9. (Currently amended) The circuitry according to claim [[7]] 1, further comprising:

an NMOS transistor M1B whose gate is connected to an input "neg", whose drain is connected to a node N10, and whose source is connected to a node N11;

a current source I1 connected to said node N11 and which is grounded;

an NMOS transistor M1A whose source is connected to said node N11, whose gate is connected to an input "pos", and whose drain is connected via a node N13 to the drain of a PMOS transistor M2A, wherein said PMOS transistor M2A has its gate connected via said node N13 to its drain, and whose source is connected to voltage VDD;

and a PMOS transistor M2B whose gate is connected to the gate of said PMOS transistor M2A, whose drain is connected to said node N10, and whose source is connected to voltage VDD;

and further comprising:

a PMOS transistor M3 whose drain is connected to a node N14, whose source is connected to voltage VDD, and whose gate PG is connected to said first stage at said node N10;

an NMOS transistor M4A whose gate and drain are connected to said node N14, and whose source is grounded;

an NMOS transistor M4C whose drain is connected to a node N16, whose gate is connected to the gate of said NMOS transistor M4A, and whose source is grounded;

an NMOS transistor M4B whose drain is connected to a node N20, whose gate is connected to the gate of said NMOS transistor M4C, and whose source is grounded;

a current source I11 one node of which is connected to a node N20, and another node of which is connected to voltage VPP;

a pair of NMOS transistors M6A and M6B whose gates are connected to each other and to node N16 via NG, and whose sources grounded, wherein the drain of said NMOS transistor M6A is connected to its gate and the drain of said NMOS transistor M6B is connected to the drain of a PMOS transistor M5A;

a current source I2 one node of which is connected to said node N16, and another node of which is connected to voltage VDD;

a pair of PMOS transistors M5A and M5B whose gates are connected to each other and to node N15 and whose sources are connected to VPP, wherein the drain of said PMOS transistor M5A is connected to its gate and the drain of said PMOS transistor M5B is connected to the output of said voltage regulator;

wherein said first stage comprises said current source I1, said transistors M1A, M1B, M2A and M2B, said second stage comprises said transistor M3, said current mirror driver and current path comprise said transistors M4A and M4B, and said first circuit comprises said NMOS transistors M4C, M6A, M6B, PMOS transistors M5A and M5B and said current source I2.